

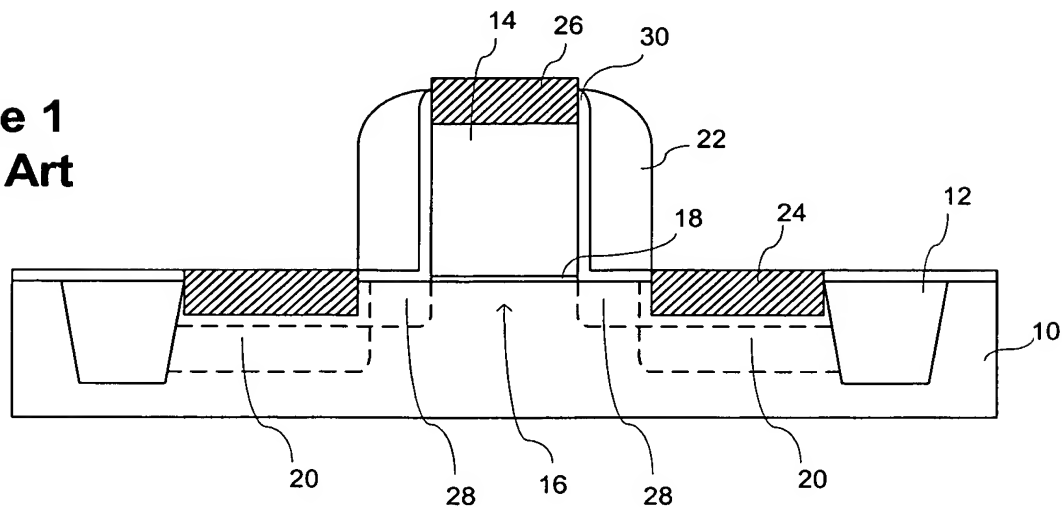
STRAINED SILICON MOSFETS HAVING NMOS GATES WITH WORK FUNCTIONS  
FOR COMPENSATING NMOS THRESHOLD VOLTAGE SHIFT

Inventors: Ihsan J. Djomehri et al. - Attorney: Ronald Coslick - 039153-0688

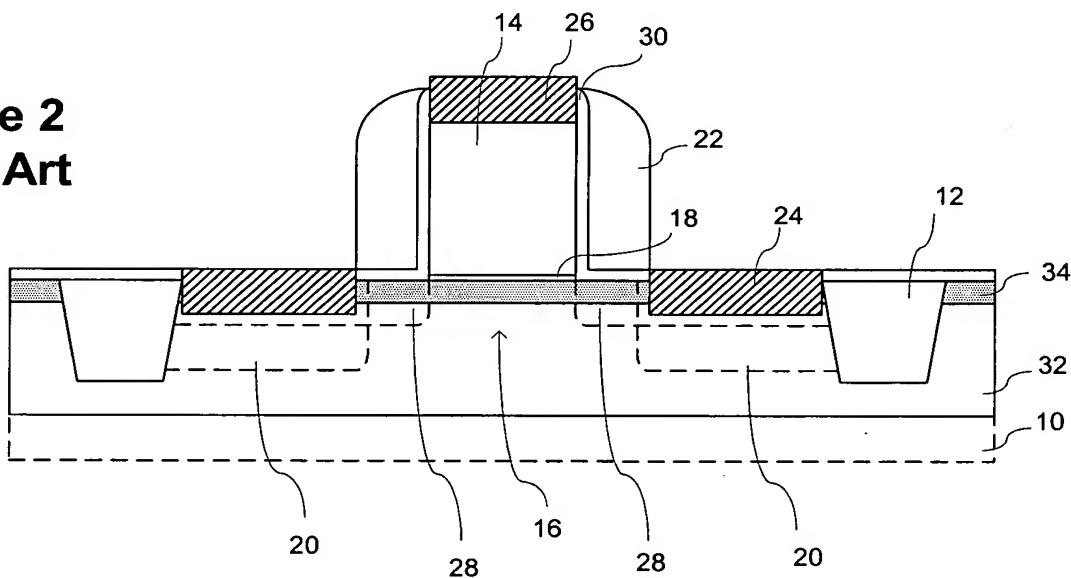
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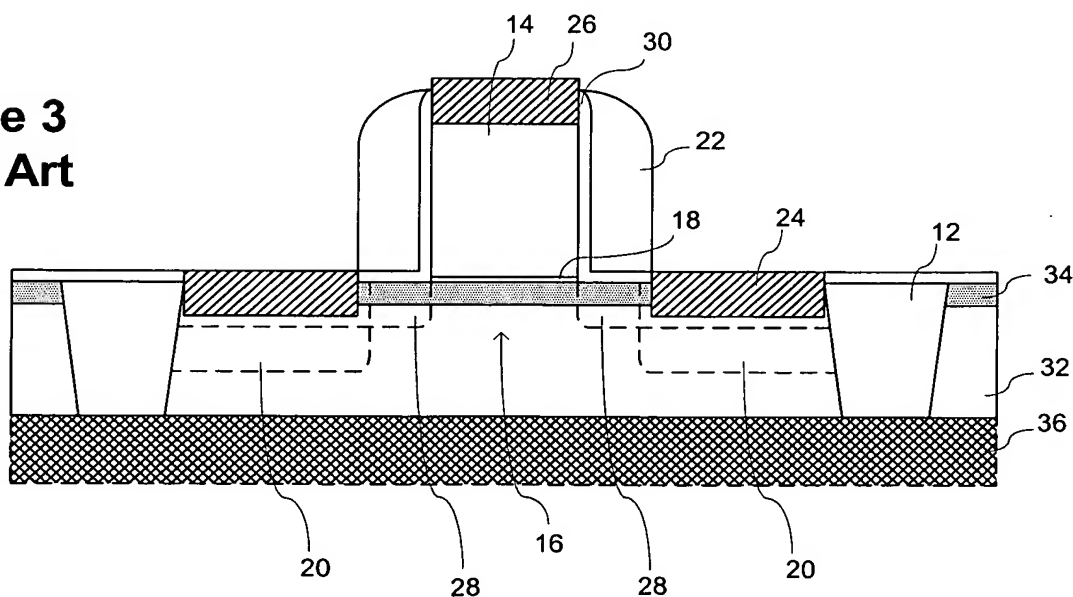
**Figure 1**  
**Prior Art**



**Figure 2**  
**Prior Art**



**Figure 3**  
**Prior Art**

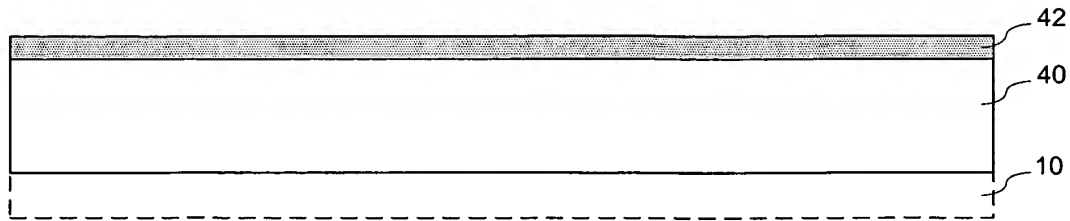


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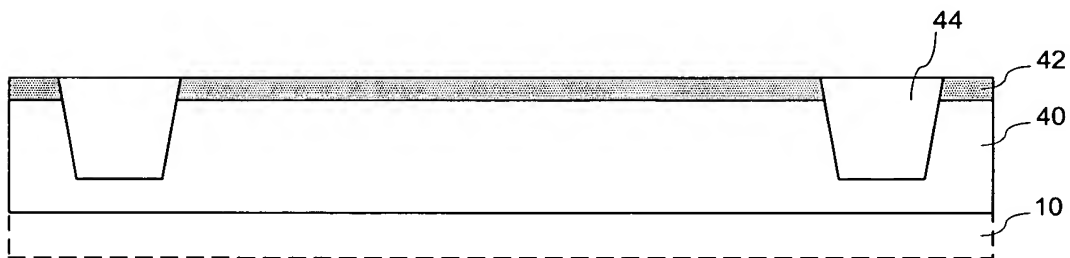
Inventors: Ihsan J. Djomehri et al. - Attorney: Ronald Coslick - 039153-0688

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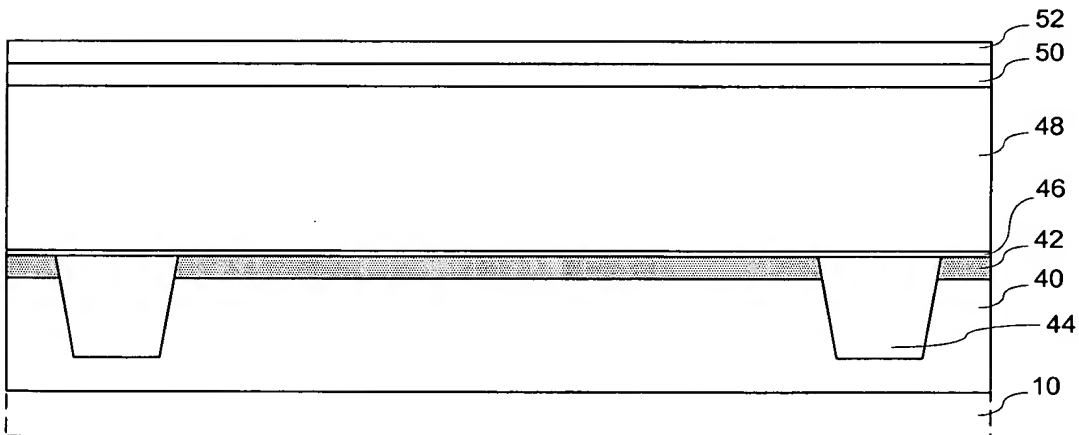
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**Figure 4a**



**Figure 4b**



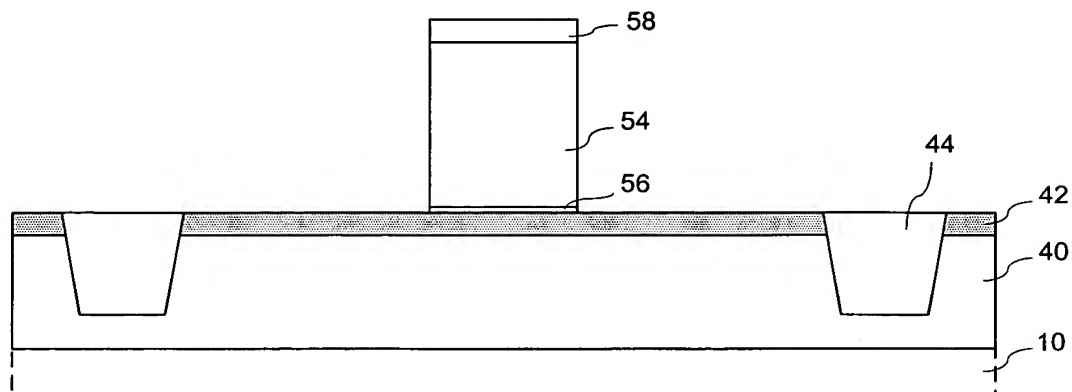
**Figure 4c**

STRAINED SILICON MOSFETS HAVING NMOS GATES WITH WORK FUNCTIONS  
FOR COMPENSATING NMOS THRESHOLD VOLTAGE SHIFT

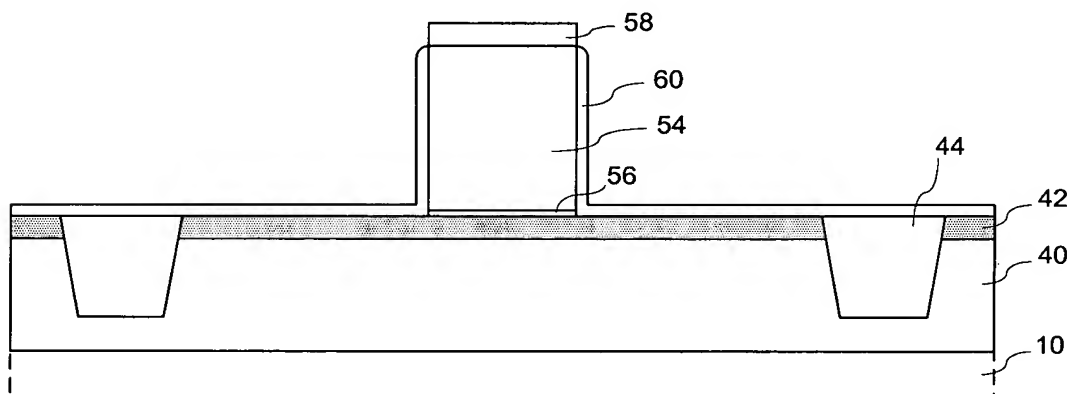
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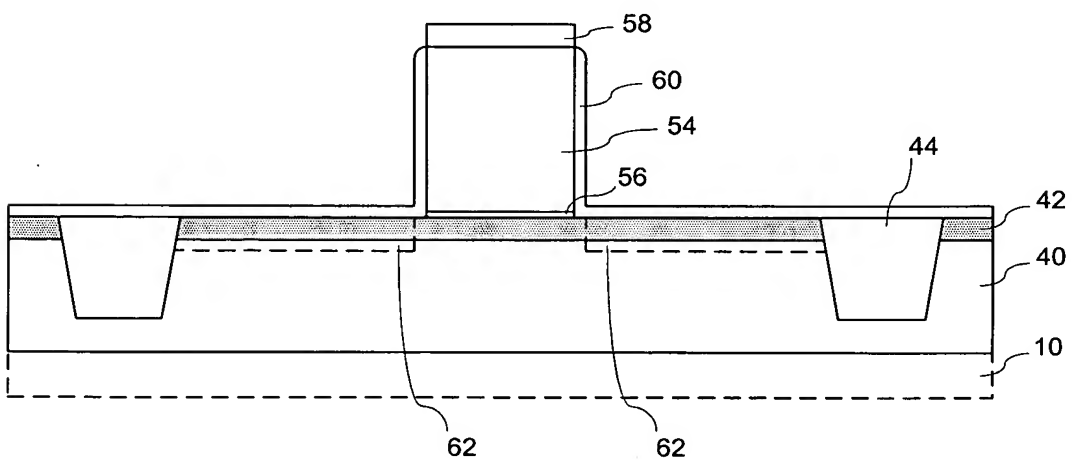
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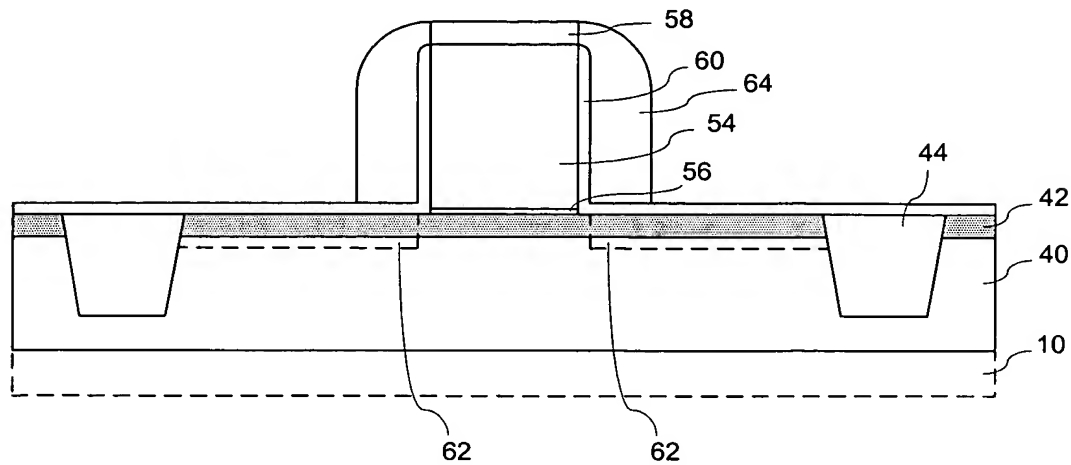
**Figure 4d**



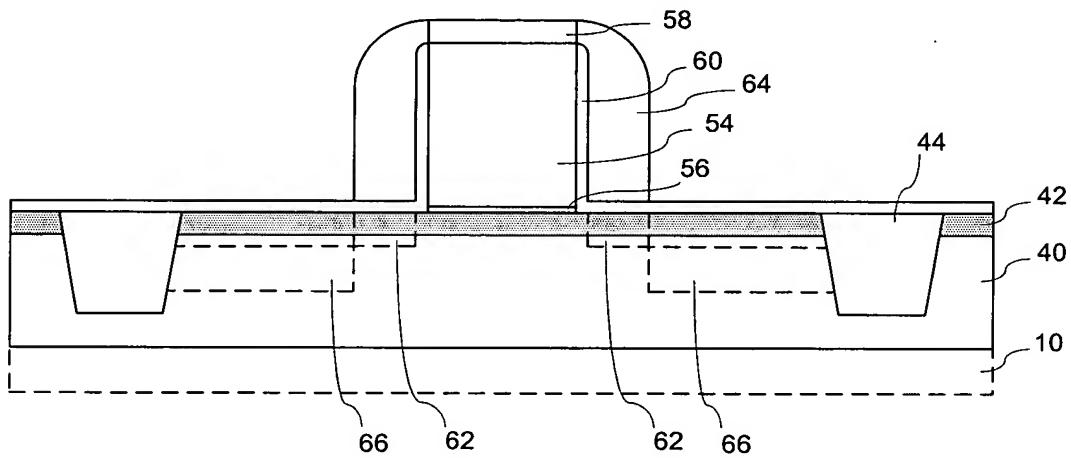
**Figure 4e**



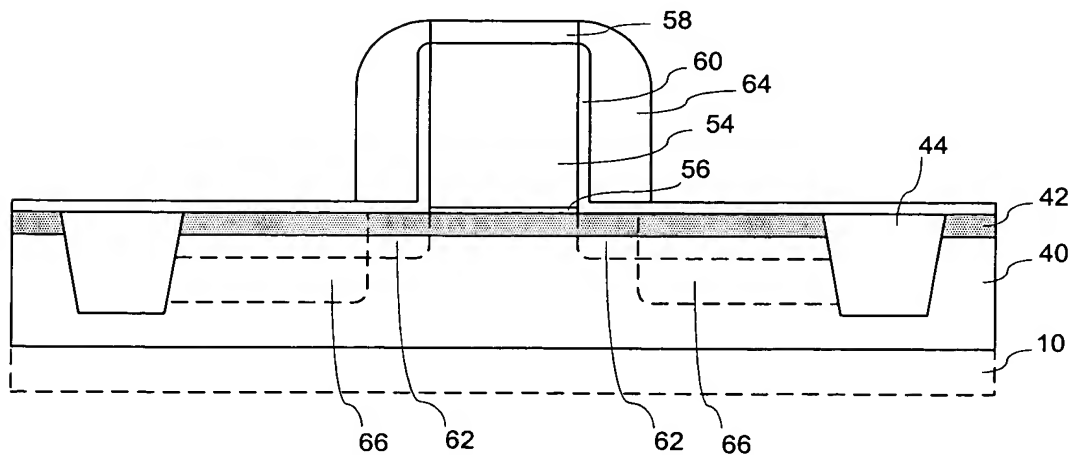
**Figure 4f**



### Figure 4g



### Figure 4h



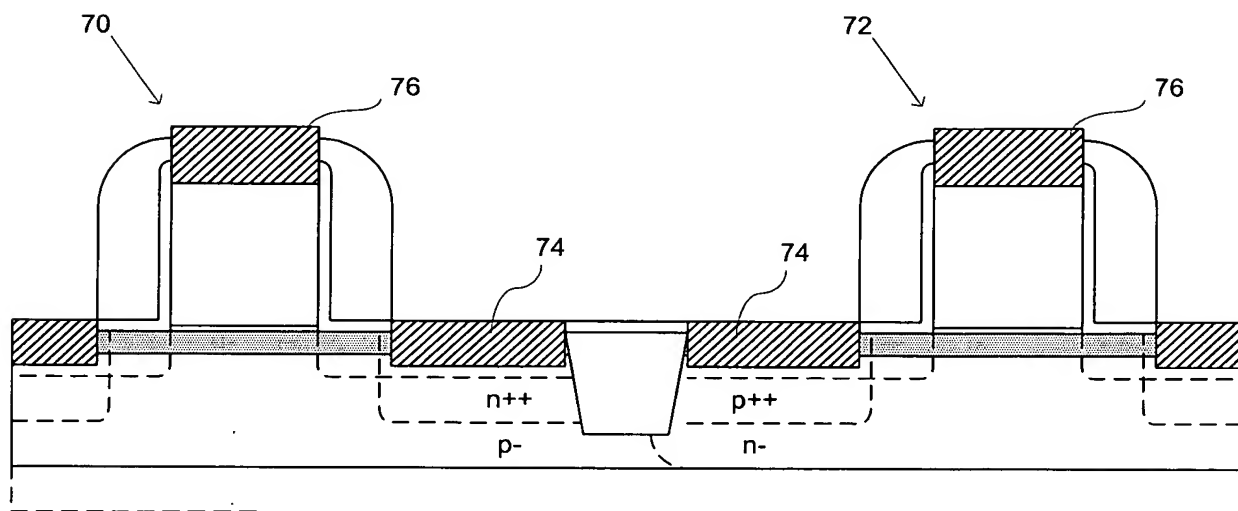
### Figure 4i

STRAINED SILICON MOSFETS HAVING NMOS GATES WITH WORK FUNCTIONS  
FOR COMPENSATING NMOS THRESHOLD VOLTAGE SHIFT

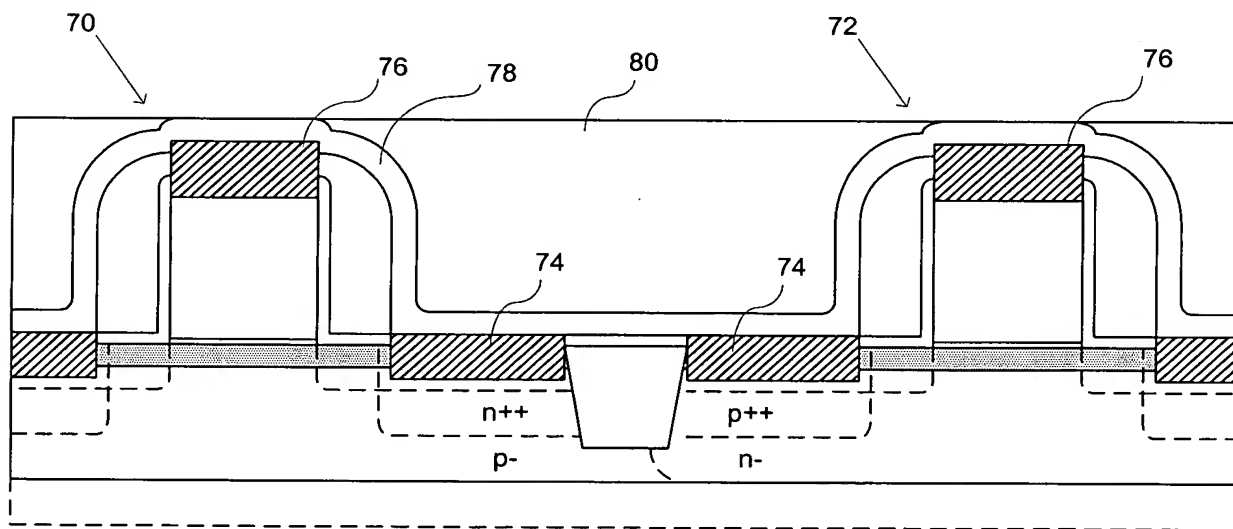
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**Figure 5a**



**Figure 5b**

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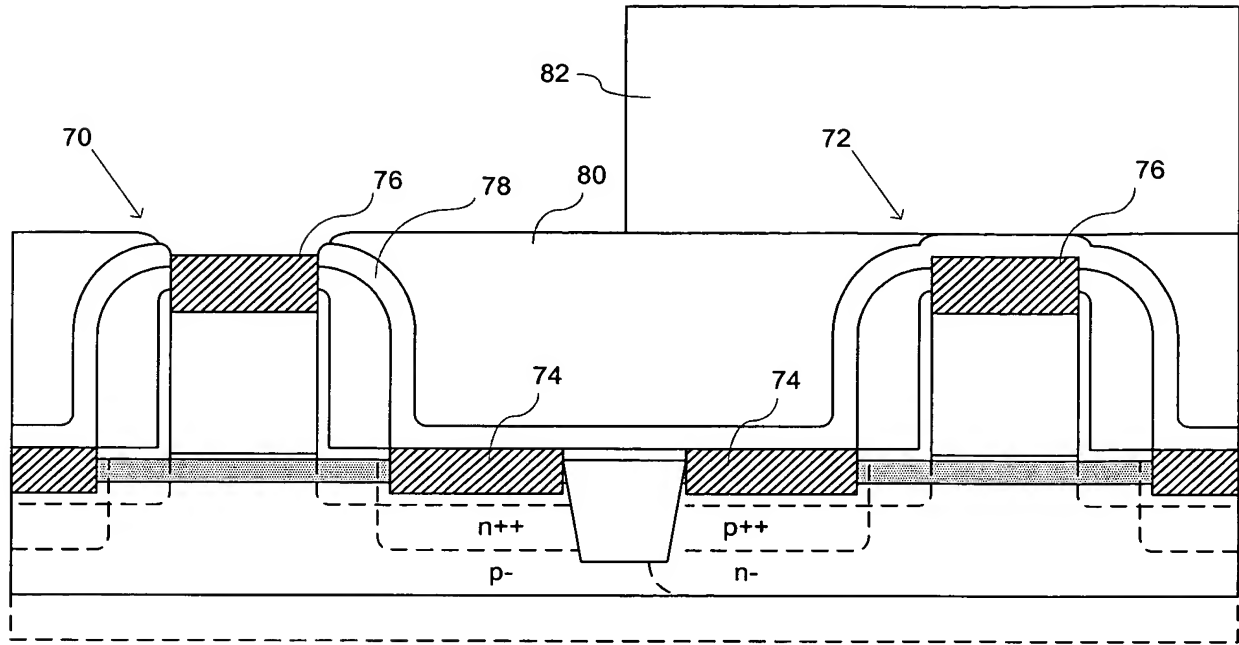


Figure 5c

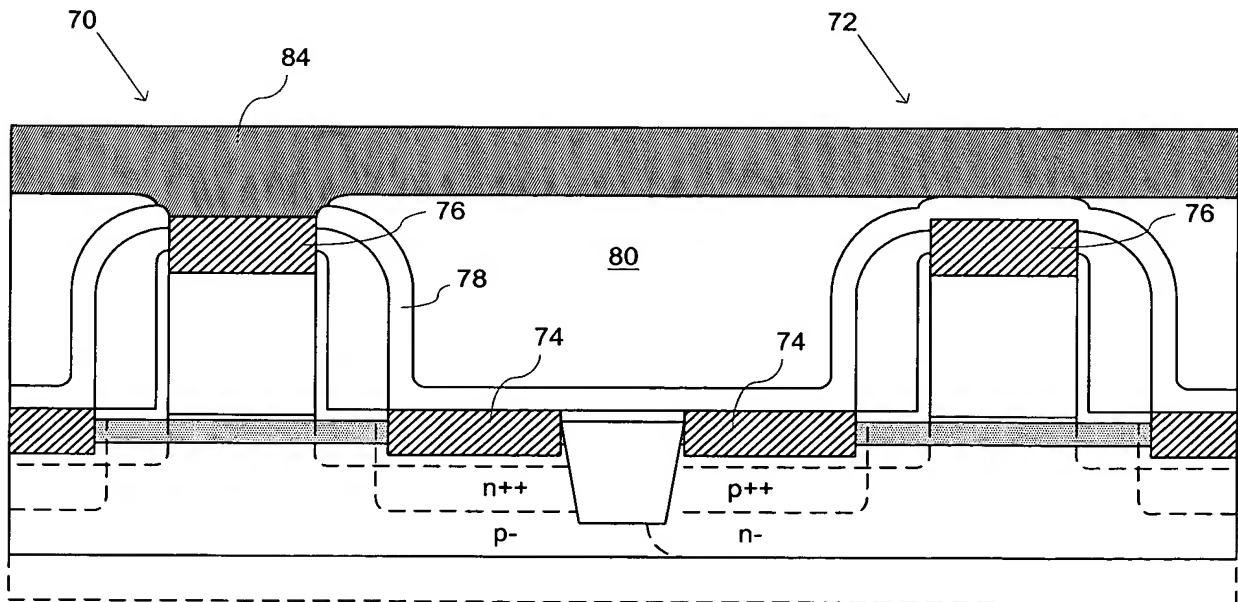


Figure 5d

STRAINED SILICON MOSFETS HAVING NMOS GATES WITH WORK FUNCTIONS  
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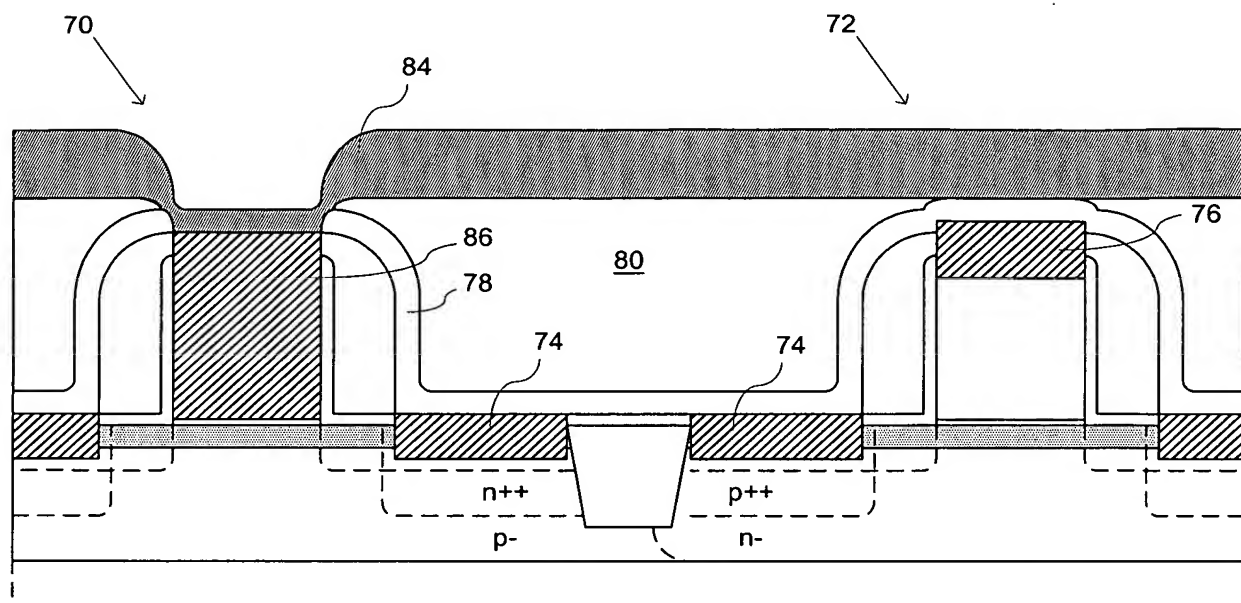


Figure 5e

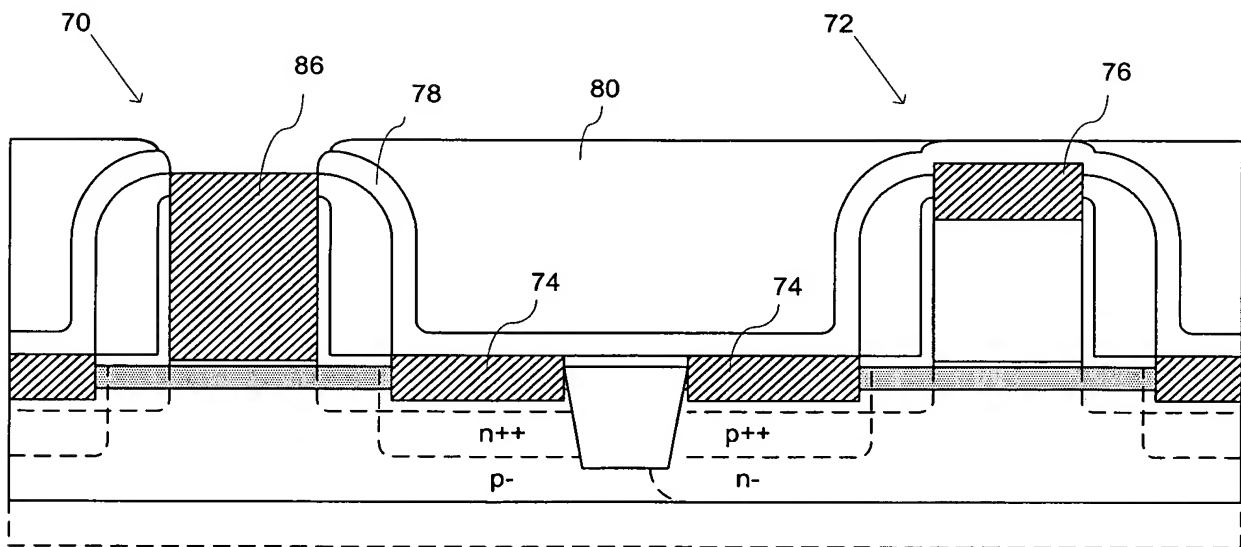
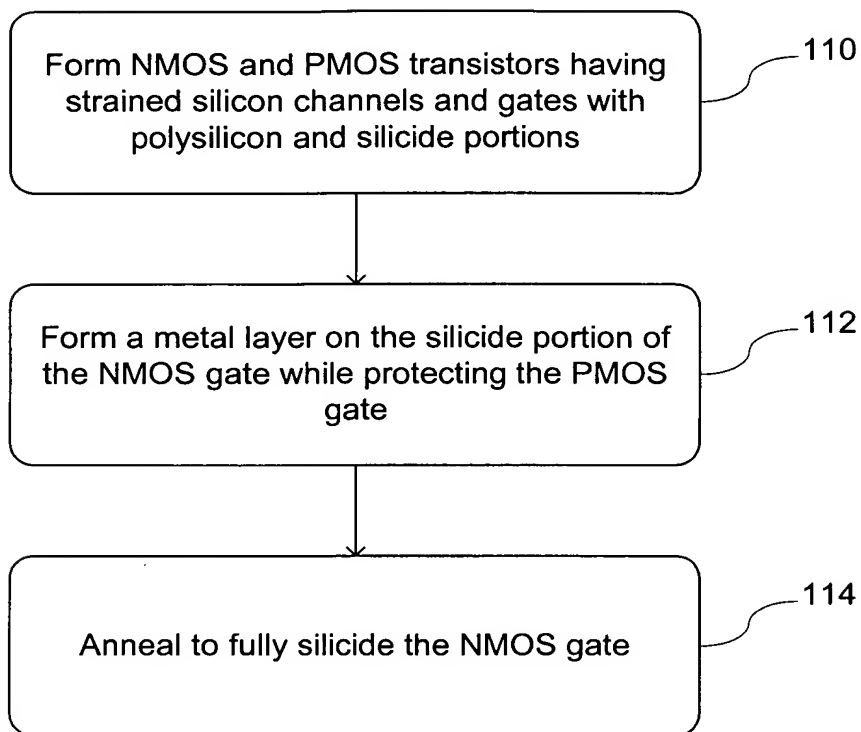


Figure 5f



**Figure 6**

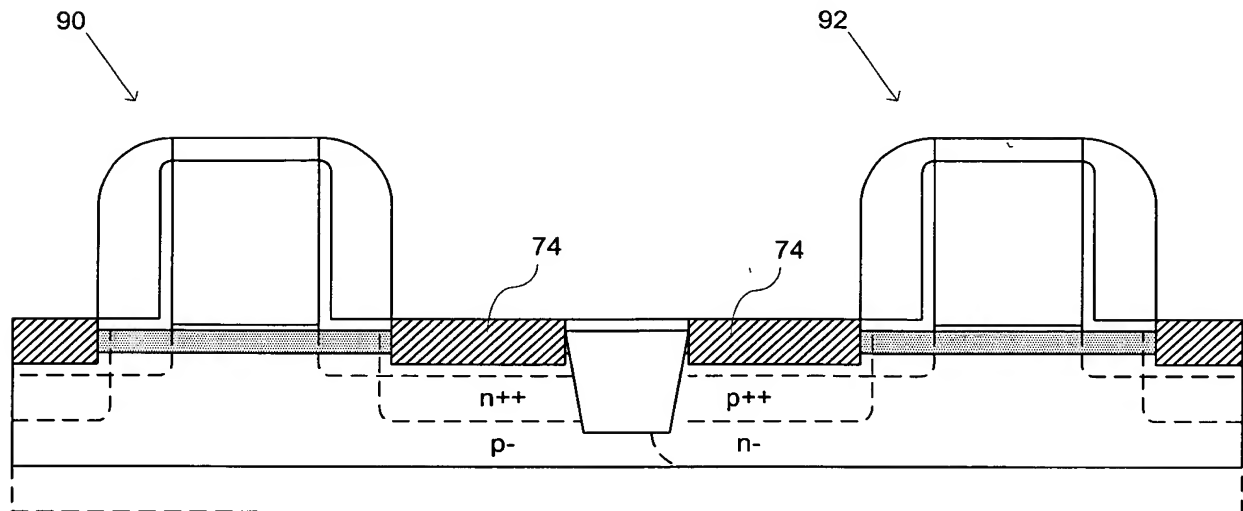


STRAINED SILICON MOSFETS HAVING NMOS GATES WITH WORK FUNCTIONS  
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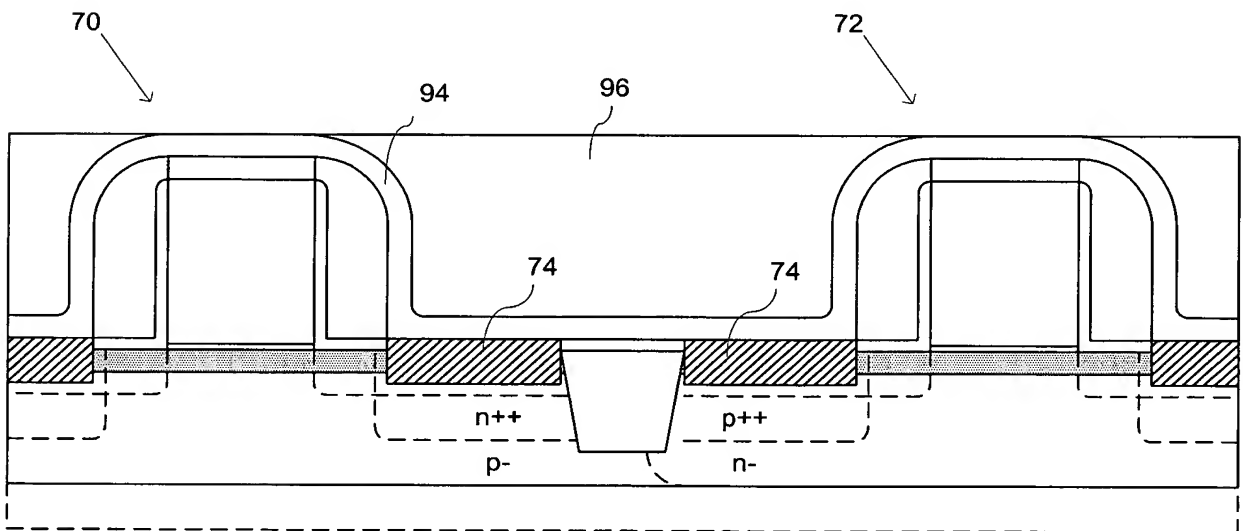
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**Figure 7a**



**Figure 7b**

STRAINED SILICON MOSFETS HAVING NMOS GATES WITH WORK FUNCTIONS  
FOR COMPENSATING NMOS THRESHOLD VOLTAGE SHIFT

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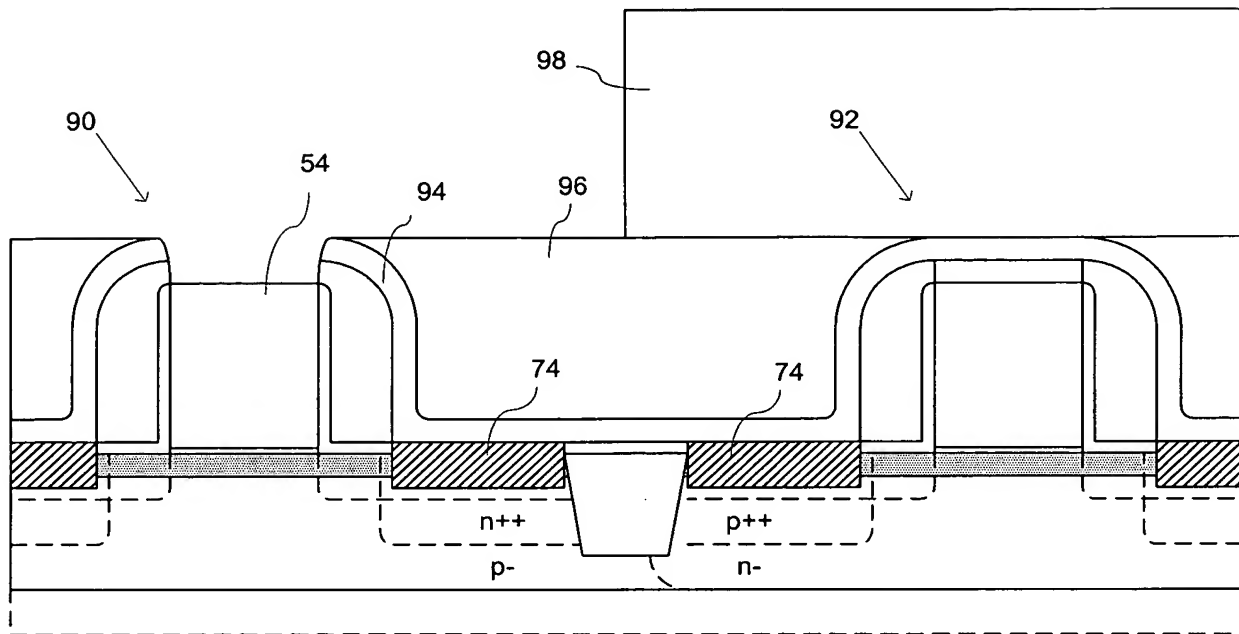


Figure 7c

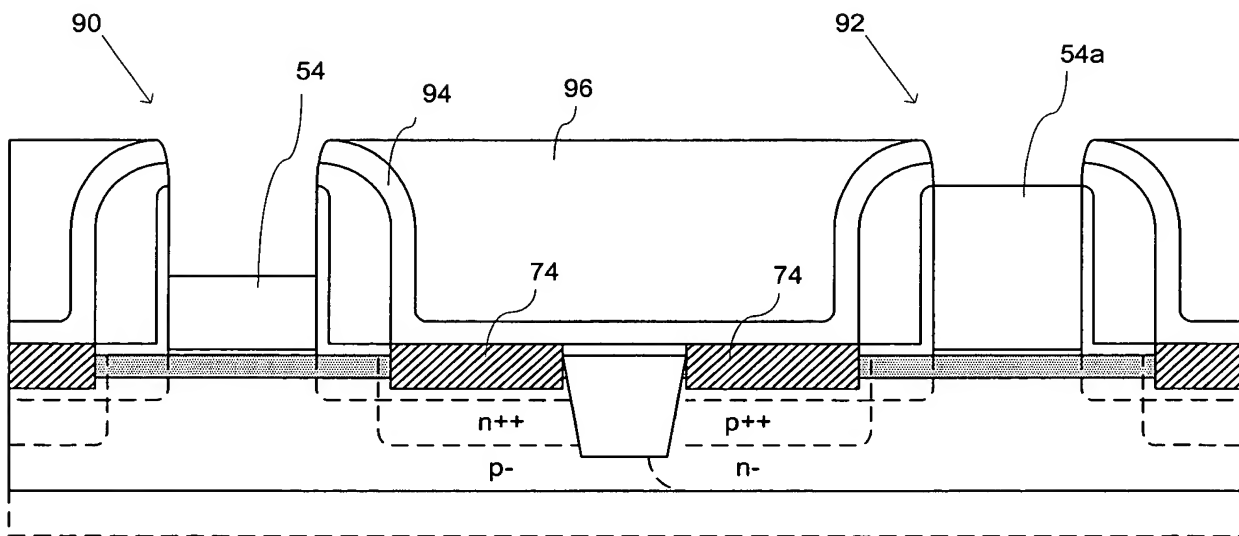


Figure 7d

STRAINED SILICON MOSFETS HAVING NMOS GATES WITH WORK FUNCTIONS  
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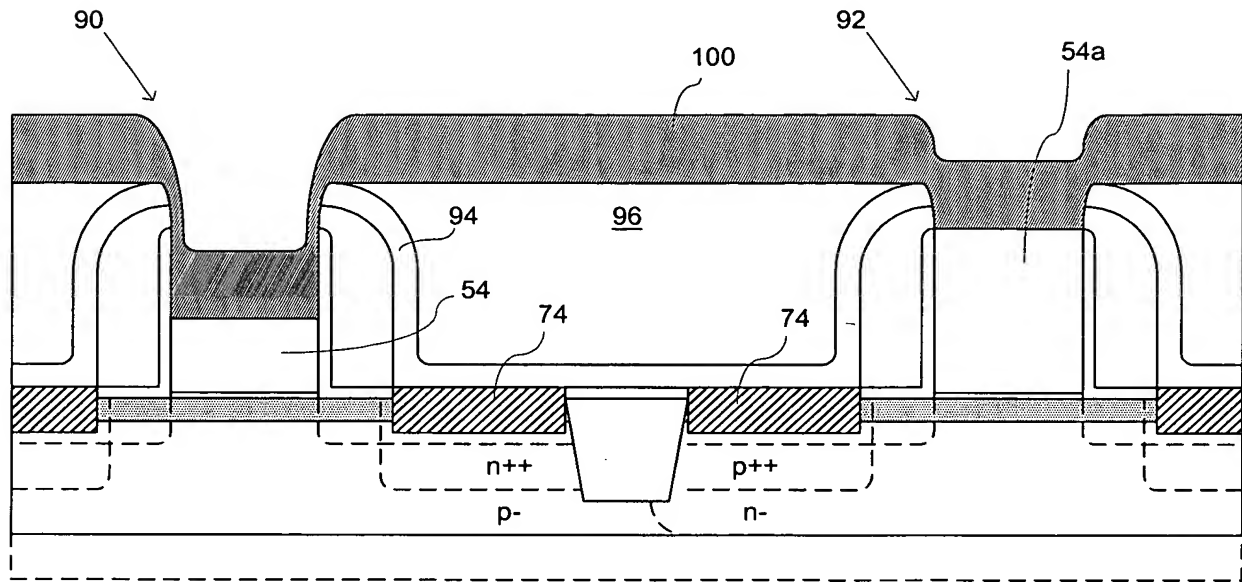


Figure 7e

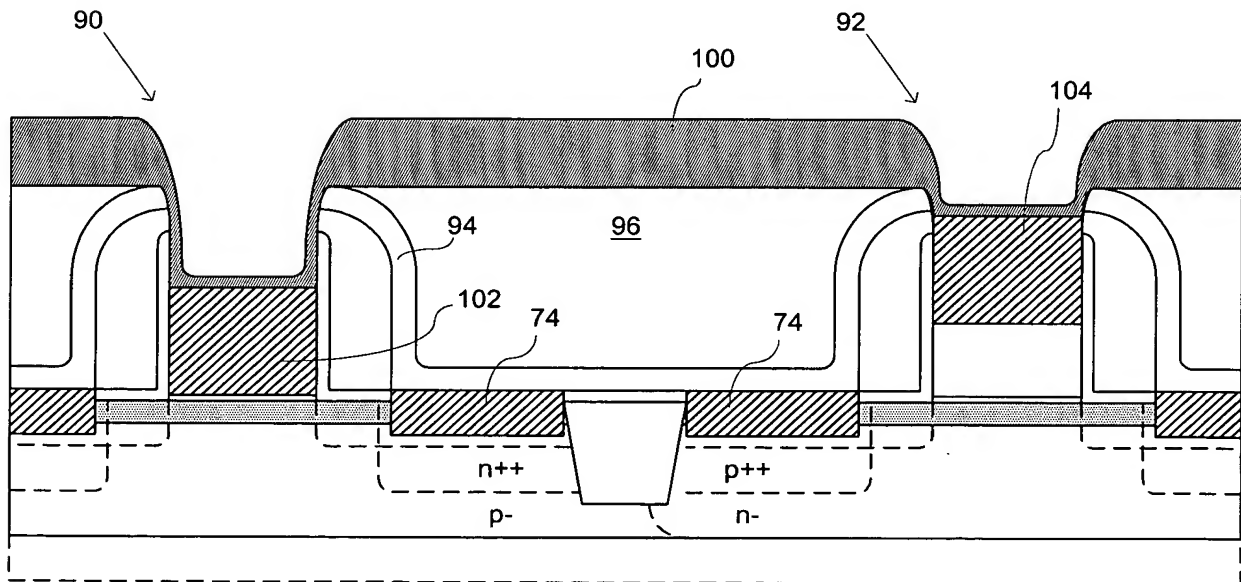
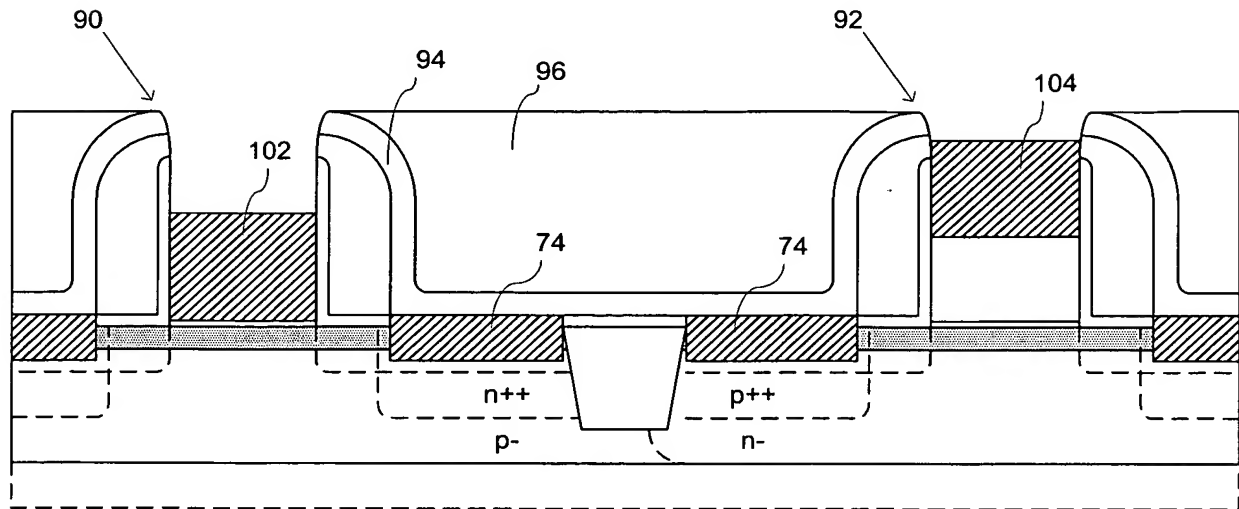
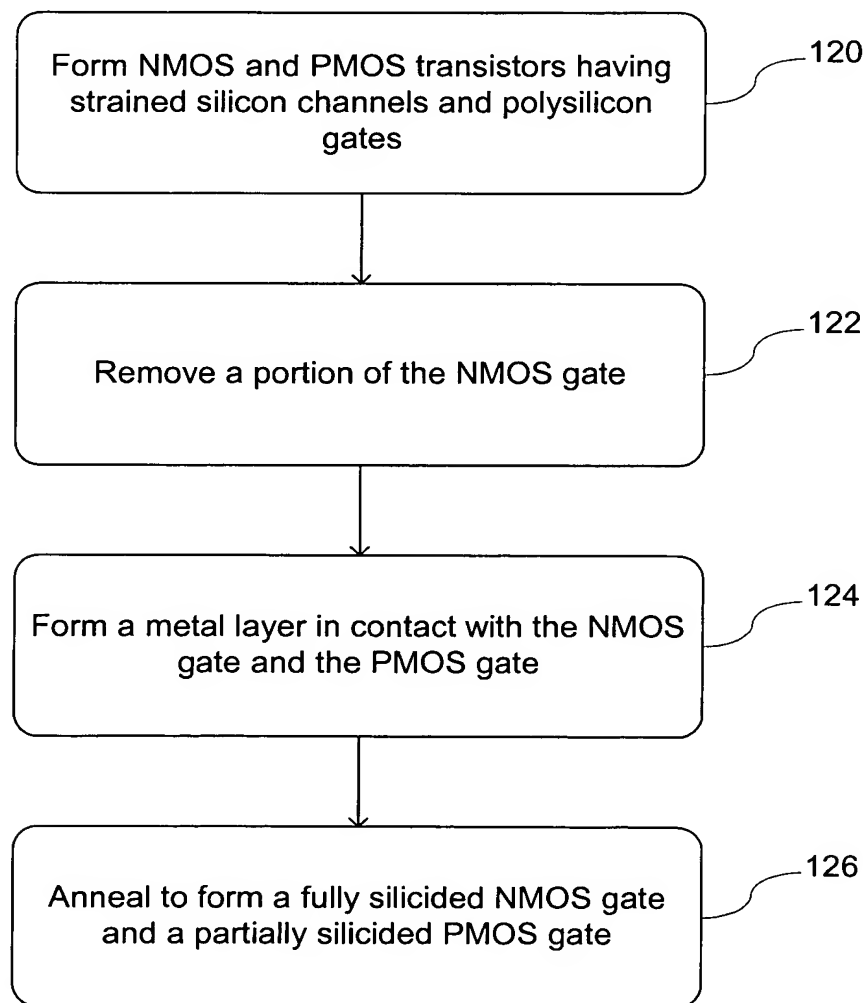


Figure 7f



**Figure 7g**



**Figure 8**

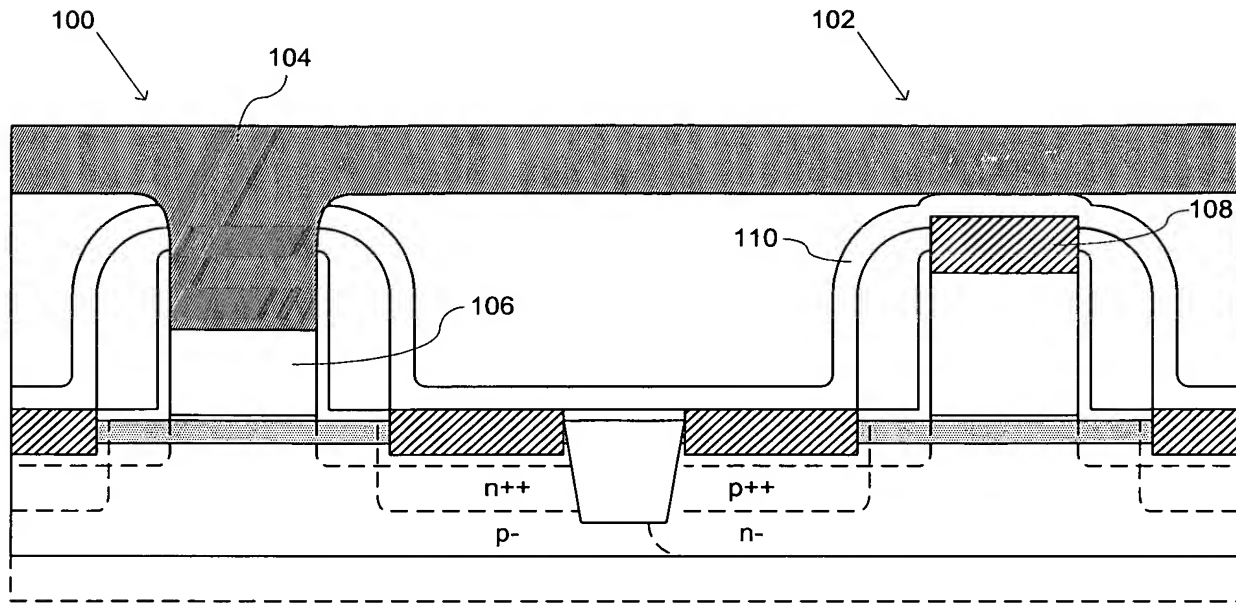


Figure 9

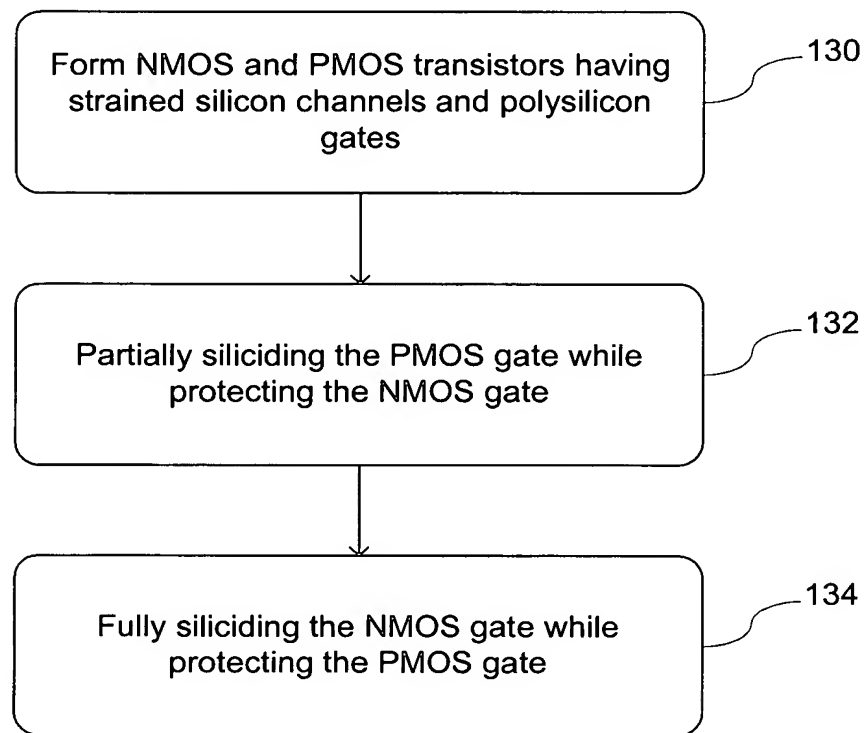


Figure 10